CLAIMS:

1. A method of reducing delays in an analogue simulation model of a hardware circuit comprising the steps of:

stimulating via an input an output of said analogue model, said output and said input having a relatively high resistance therebetween; and

applying a pulse to a relatively low resistance, whereby when said pulse is applied to the relatively low resistance, the input is connected to said output via the relatively low resistance so that the time constant of the circuit is reduced.

2. A method as claimed in claim 1, wherein the relatively high resistance is connected in parallel with the relatively low resistance.

3. A method according to claim 1 or 2, wherein in said step of applying a pulse, the output is connected to a voltage source having a high drive strength for the duration of the pulse and the voltage source is disconnected before the pulse has time to propagate through the circuit attached to said output.

4. A method according to any of claims 1 to 4, further comprising the steps of:

applying a voltage to said input, which is applied to said output via the relatively high resistance to apply a test voltage having a weak drive strength to the output.

5. A method according to claim 4 further comprising the steps of:

providing a delay element operable to provide a delayed control signal and responsive to said delayed control signal disconnecting said relatively low resistance from between the input and said output.

6. A method according to any one of claims 1 to 5, in which said analogue model is stimulated with an expanded standard logic package.

7. A method as claimed in claim 6 wherein said method is used when a Z state is present.

8. A method according to any preceding claim, in which said relatively high resistance has a resistance of between 500 kilo ohms and 1.5 mega ohms.

9. A method according to any preceding claim, wherein said relatively low resistance has a resistance of between 0.5 ohms and 10 ohms.

10. A method according to any one of claims 1 to 9, in which said pulse has a duration of between 50 pico seconds to 150 pico seconds.

11. A method as claimed in any preceding claim, wherein said analogue model is a SPICE model.

12. A system for reducing delays in an analogue simulation model of the hardware circuit comprising:-

means for stimulating via an input an output of the analogue model, said output and said input having a relatively high resistance therebetween; and

means for applying a pulse to a relatively low resistance, whereby when said pulse is applied to the relatively low resistance, the input is connected to said output via the relatively low resistance so that the time constant of the circuit is reduced.

13. A computer program comprising code means for performing any of the steps of any of claims 1 to 11 when the program is run on a computer.